[This question paper contains 5 printed pages.]

6636 *Your Roll No.....*

**B.Sc. (Hons.) Computer Science / II Sem. B**

Paper CSHT-204 : Computer System Architecture

(Admissions of 2011 and onwards)

*Time : 3 Hours* *Maximum Marks : 75*

*(Write your Roll No. on the top immediately on receipt of this question paper.)*

*Question No.* **1** *is compulsory.*
*Attempt any* **four** *questions from Section* **B.**
*Parts of a question must be answered together.*

## SECTION – A

1. (a) The memory unit of computer has 256K words of 32bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of 7 addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field. (5)

   (b) Derive the speedup factor for a n-instruction, k-stage instruction pipeline ? How many clock cycles would the 10th instruction take to complete in a 6-stage pipeline ? (5)

P.T.O.

(c) List the micro operations for executing BSA and ISZ micro instructions. (5)

(d) What is the purpose of a pseudoinstruction ? Give three examples of pseudoinstructions. (5)

(e) What are the characteristics of RISC and CISC processors? How is RISC processor better than a CISC processor ? Justify your answer. (5)

(f) The control memory has 2048 words of 32 bits each. Each microinstruction has three fields. Three micro operations are specified by 15 bits. (5)

(i) How many bits are there in the control address register ?

(ii) How many bits are there in the branch address field and the select field ?

(iii) If there are 8 status bits in the system, how many bits of the branch logic are used to select a status bit.

(iv) How many bits are left to select an input for the multiplexers.

(v) Draw the microinstruction code format showing all fields.

(g) (i) Distinguish between memory mapped I/O and the Isolated I/O. (3)



(ii) List two differences between write-through method and the write-back method for updating the main memory. (2)

## SECTION – B

2. (a) With the help of a flowchart and an example, explain interrupt cycle. (6)

(b) Design the control gates associated with the address register (AR) in basic computer with the following register transfer statements :

$R'T_0 : AR \leftarrow PC$

$R'T_2 : AR \leftarrow IR(0\text{–}11)$

$D'_7 IT_3 : AR \leftarrow M[AR]$

$RT_0 : AR \leftarrow 0$

$D_5T_4 : AR \leftarrow AR+1$ (4)

3. (a) What micro operations are required for executing branch unconditional (BUN) instruction. (3)

(b) If total memory space accessed by the central processing unit is 32K, how many bits are required in its program counter ? (2)

(c) Explain read and write cycles for the synchronous and asynchronous bus operations with the help of timing diagrams. (5)

P.T.O.

4. (a) Formulate a mapping procedure that provides sixteen consecutive micro-instructions of each routine of a typical computer. The operation code has six bits and the control memory has 2048 words. (4)

(b) Draw the block diagram of microprogram sequencer for control memory, and explain its working with the help of truth table. (6)

5. (a) An instruction is stored at location 100 with its address field at location 101. The address field has the value 500. PC has the value 100. A processor register R1 contains the number 300 and content of index register is 200. Evaluate the effective address and operand if the addressing mode of the instruction is (All values are in decimal) :

(i) Direct

(ii) Immediate

(iii) indirect

(iv) Relative

(v) Register indirect

(vi) Index with R1 as index register (6)



(b) Convert the expression (3+4)* [10* (2+6) + 8] into RPN (postfix notation) and show stepwise the stack operations for evaluating the numerical result. (4)

6. (a) Describe with the help of block diagram how multiple matched words can be read out from an associative memory. (6)

(b) A two-way set associative Cache memory uses blocks of four words. The Cache can accommodate a total of 2048 words from main memory. The main memory size is $128K \times 32$. What are the sizes of the :

(i) TAG

(ii) INDEX

(iii) DATA

(iv) Cache memory (4)

7 (a) Give block diagram of DMA controller. How does CPU initialize the DMA transfer ? (5)

(b) What is program controlled I/O ? What is Interrupt driven I/O ? Outline the disadvantages of program controlled and Interrupt driven I/O. (5)